



#### SIGNAL INTEGRITY ANALYSIS WITH ALTAIR POLLEX™ DDR DESIGN CASE

DaiHo Ham (daiho@altair.com), Dr Jordi Soler (jsoler@altair.com) - Sept 25, 2020

### Outline

- 1. Introduction
- 2. DDR Design Case Study
- 3. Benchmark study
- 4. Summary



### **1. Altair PollEx**

Altair PollEx is a PCB level EDA software suite available under Altair Units covering PCB design review, verification, analysis and manufacturing, to significantly reduce development cycles while providing a common application for schematic engineers, PCB designers, CAE analysts and manufacturing engineers to communicate





### **1. Altair Pollex Customer Base**

- Strong customer base with global customers and a leading position in South Korea
- Leading players with top level e-manufacturing technologies, including Samsung and LG, using PollEx

🚯 LG Electronics	SAMSUNG MISHONGS	🕞 LG Electronics	ADVANTEST.	Dynatron	Canon	📕 🚯 LG	Uni Test	LENECO
LG MC / DM / DD / DA Division	SAMSUNG Electronics	LO PERI	ADVANTEST CORPORATION	Dynatron Co.17D.	Canon Korea	Encason-LG Enlerprise Co., LM	Unified Inc.	LENECO Co., LM
CAMERINE SAMERAN	CARLEND LANDAG IN	KEFICO	NISSAN	SANYO	😹 kyungshin	SIEMENS	Microfriend	<b>OGMIF</b>
SAMSUNG Electro Mechanica	SAMSUNO SDI	HYUNDAI KEPICO	NISSAN MOTOR CO.,LTD.	SANYO	Kyungahin	Samara (M	Address and the	Websighter Providence
🙆 Hanwha Techwin	STREET SALES	ETRI	SL Corporation	S Komtec		HYEJEON COLLEGE	Sau 신안산대학교	KORENTECH
Harwha Techwin	SAMSUNG Heavy Industries	Electronics and Telecommunication Research Institute	SL Corporation	Kantec	OMRON AUTOMOTIVE ELECTRONICS KOREA CO., LTD	mit won course	She was University	Rosea University of Technology & Education
<b>G</b> nfinental S	ANNERS SAMELING DEPLAY	A MANDO	QUALCOMM	(intel)	MEXELL	NAVER	Cafeel	HYOSUNG TNS
Continental Automotive Systems Corporation	SAMSUNG Depley	MANDO Corporation	Qualcomm	Intel Corporation	Nexel Co.1.M.	SAIDS CHE	PMB Cal. LTD.	Radius Hymeng
lauraix		A	BIXOLON'	Clonotek	DAESUDO	15 Automation	SHL37-2	Incr
riding	U Display		BIXOLON	See and a second	U DAESUNO	Planation of the	BYRTEK Carboniza	MARDING-To. 18
Hyrix Semiconductor	LG Deplay Co. LM.	HYUNDAI MOTOR COMPANY	Birsten Co.1.M.	LG involte: Co.LM.	Deesung Electronic Co., LM.	Lt Automation Techningers	BTETEC Coperation	Matantas In. 18 Matantas Inc.
	LO Display		Boolan Co. LM	LG involte Co.LM	Declaring Electronic Co., LM.		SONY	Meadourius Panasonic
Provis Teensonductor MOBIS Providei Autonet	La Display La Display Co. Lil Karea Electronica Technology Installes (2017)		Broten Ca.LM.	KUMHO HT Inc.	Consung Electronic Co., LM.	It Adams Schenges NEC NET Pattern Lik	TITEC Coperation SONY	Mandola N. M Mandola Tha Panasonic Persona Capacita
Proc Lanceonductor MODELS Process Automet	LO Deservice Juli Konstantioner Stationers Konstantioner Stationers HUMAX	нтински коток сомики НТИПОН ИТИПОН ТОГОРАС	Brother Co. LM Mendo-Hells Electronics Corp. LEDLITEK		Diresund Dereng Bectron Co. LM Suprime Suprime		Constants	Panasonic Panasonic Persent Capation Dreamus
Pyre tamonduse Pyre tamonduse MOBIS Pyunda Aateur Concerned	LO Deskey Co. J.M. LO Deskey Co. J.M. Keinen Statussey Ke	ичиван коток сомянич нушван коток сомянич нушван литвон учиван литвон тораz тораz	Evoluti Co. J.M. Mando-Hella Electronica Corp. LEDLITEK LEDLITEK (co. J.TO.	LO HUNDLEK LE HUNDLE CO.LM KUMHO HT Inc KUMHO HT Inc VURA Cognition	September Co. LM.		ETTEC Conserver ETTEC Conserver SONY Expression Expression EXPRESSION EX	Material for the second
Inter Semendarian Models Pyreter Autorer Senerce SHARP	LO Deplay Ce JAI Kepton Restances Intensing HUMAX Indust Name Indust Name	нтинсы коток сомями нтипси сомями нтипси истехно нтипси истехно точка со., сто сона со., сто сона со., сто сона со., сто сона сона сона сона сона сона сона сона	Bendem Ca. J.M.	EXAMPLEER LE Involve: Co.LM KUMHO HT NUMHO HT Inc. VURA Corporation: Hansol	Sepresa Section Sepresa Kacimana Ge, LM MYUNDAR		TOTAL CARANA TITUES Conversion SOONY Conversion Co	Material State



# **1. Introduction**

PollEx Signal Integrity (SI)

The goal of SI in PollEx is to obtain the best signal quality by analyzing and adjusting multiple factors, including:

- Reflection due to impedance discontinuity, crosstalk, jitter due to Inter Symbol Interference (ISI)
- SI power and ground bounces, trace and via stubs, trace cross over plane split, improper signal return path, transmission line loss, improper net topologies
- Differential pair length mismatch , power distribution network problem, via parasitic, bus nets length mismatch, line delay difference between M/S and S/L structure, driver fan in/out, signal edge rate, trace self resonance, part to part skew





#### Description

- CPU (U1) drives signal into two memories (U204, U205)
- Operating Speed: DDR3\_1066 AC175
- Drive strength: 30 mA
- Termination: None
- Topology: Tree topology (unbalanced and distributed)
- Impedance: Mismatched







### Problem to Solve

- The "Eye" is closed, and thus data communication is not possible
  - Overshoot / ringback is large due to the reflection noise caused by the impedance discontinuity
  - Timing skew exists between two memories caused by the unbalanced branch length.
  - Big jitter due to the Inter Symbol Interference (ISI)
  - Possibility that the ringback will be larger due to crosstalk or power noise.
  - The branch length is long, so it works as a distributed load.



![](_page_6_Picture_10.jpeg)

#### Improvement 1

**Improvement -** Added Thevenin type termination to reinforce impedance mismatch problem

![](_page_7_Figure_4.jpeg)

**Results -** Decreased overshoot and opened Eye. However, the cyan colored improved waveform still touches the eye-mask

![](_page_7_Figure_6.jpeg)

![](_page_7_Picture_7.jpeg)

Improvement 2

**Improvement -** Adjusted to the same branch length of loads and changed to lumped load topology

![](_page_8_Picture_4.jpeg)

**Results -** Improved voltage / timing margin (cyancolored waveform)

![](_page_8_Figure_6.jpeg)

![](_page_8_Picture_7.jpeg)

**Improvements 3** 

**Improvement -** Modified the layer stack up to reduce the gaps between the net and the reference plane

![](_page_9_Figure_4.jpeg)

**Results -** Reduced FEXT amplitude (cyan-colored waveform)

![](_page_9_Figure_6.jpeg)

![](_page_9_Picture_7.jpeg)

Results

- Significant improvements in the design by applying the three changes
- Improved voltage margin up to 400mV and timing margin up to 630pS/779pS (setup / hold)

![](_page_10_Figure_5.jpeg)

![](_page_10_Picture_6.jpeg)

### Single-Ended Case - Description

- CPU(U1) drives signal into memory (U204)
- Operating speed: DDR3\_1066 AC175
- Drive strength: 60Ω (17.4 mA)
- Receiver termination: 120Ω Thevenin
- Topology: Point to point topology
- Ground condition: Ideal ground
- Bit Pattern: Periodic

![](_page_11_Figure_10.jpeg)

![](_page_11_Picture_11.jpeg)

![](_page_11_Picture_12.jpeg)

#### Single-Ended Case – S Parameters Results

![](_page_12_Figure_3.jpeg)

Resonant frequencies are identical

٠

 Amplitude at resonant point is slightly different but being this difference acceptable

![](_page_12_Picture_6.jpeg)

### Single-Ended Case – Eye Diagram and Waveform Results

![](_page_13_Figure_3.jpeg)

- Overshoot / ringback positions and quantities are identical
- The amplitude at each point is slightly different, but since the trend of the signal waveform is consistent, this degree of error can be tolerated

![](_page_13_Picture_6.jpeg)

### **Differential Line Case – Description**

- CPU(U1) drives differential signal into memory (U204)
- Operating speed: DDR3\_1066 AC175
- Drive strength: 60Ω (17.4 mA)
- Receiver termination: 120Ω
- Topology: Point to point
- Ideal ground
- Bit pattern: Periodic

![](_page_14_Figure_10.jpeg)

![](_page_14_Picture_11.jpeg)

![](_page_14_Figure_12.jpeg)

#### Differential Line Case – S Parameters Results

![](_page_15_Picture_3.jpeg)

- Resonant frequencies are identical
- Amplitude at resonant point is slightly different but being this difference acceptable

![](_page_15_Picture_6.jpeg)

#### Differential Line Case – Eye Diagram and Waveform Results

![](_page_16_Figure_3.jpeg)

- Overshoot / ringback positions and quantities are identical
- The amplitude at each point is slightly different, but since the trend of the signal waveform is consistent, this degree of error can be tolerated

![](_page_16_Picture_6.jpeg)

### 4. Summary

- The purpose of SI applied in early development stages is to predict signal distortion when the driver waveform reaches the receiver stage and to secure the timing and voltage margins
- We have presented a DDR design case, where the overshoot caused by impedance mismatch is large, shortening the life of the IC and creating a large ringback, which can cause system malfunction when invading the threshold area
- Enough design margins with the elements which can be controlled in advance should be provided to have a robust design where unpredictable factors that cannot be predicted do not case system failure. We have shown 3 improvements:
  - In order to reduce the overshoot caused by impedance mismatch, add the appropriate value termination
  - Adjust the topology to balance the load to minimize the effect of reflection noise skew
  - Crosstalk noise can worsen ringback, thus reduce crosstalk noise as much as possible
- Being fast and reliable, PollEx SI provides the same level of accuracy as a competing and long-established SI EDA analysis software

![](_page_17_Picture_9.jpeg)

# **THANK YOU**

altair.com/pollex

![](_page_18_Picture_2.jpeg)

![](_page_18_Picture_3.jpeg)